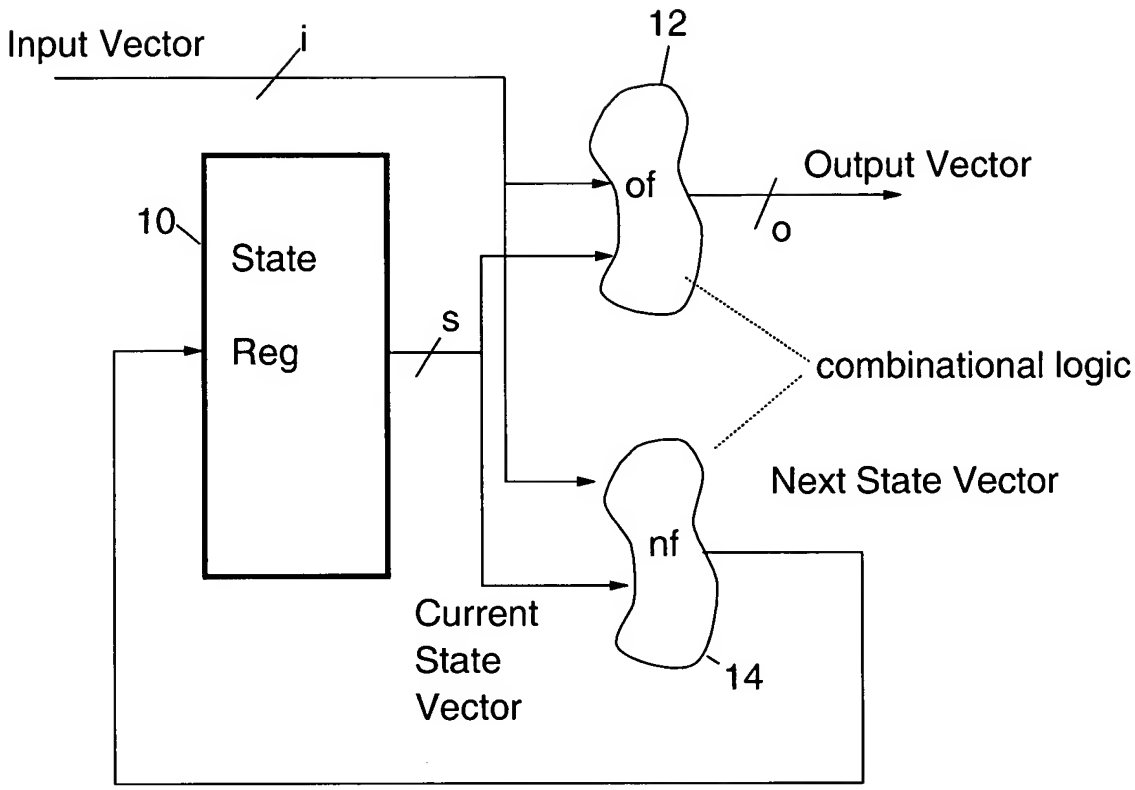


of = Output function
nf = Next State function

FIG. 1

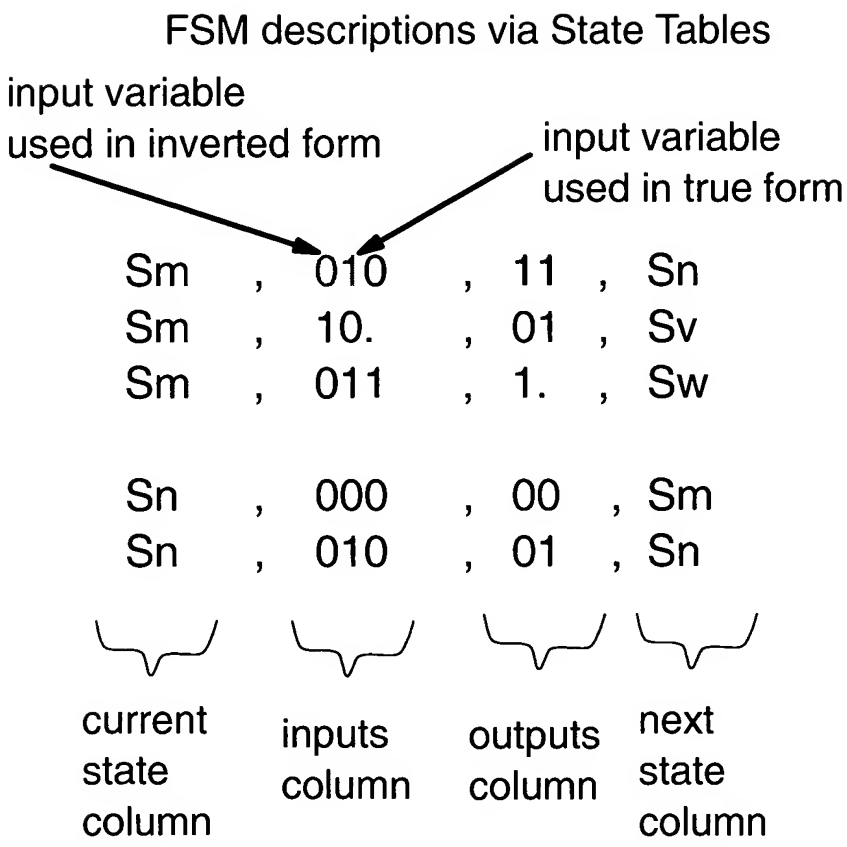

FSM descriptions via State Tables
input variable
used in inverted form
input variable
used in true form
Sm , 010 , 11 , Sn
Sm , 10. , 01 , Sv
Sm , 011 , 1. , Sw
Sn , 000 , 00 , Sm
Sn , 010 , 01 , Sn
current
state
column
inputs
column
outputs
column
next
state
column

FIG. 2

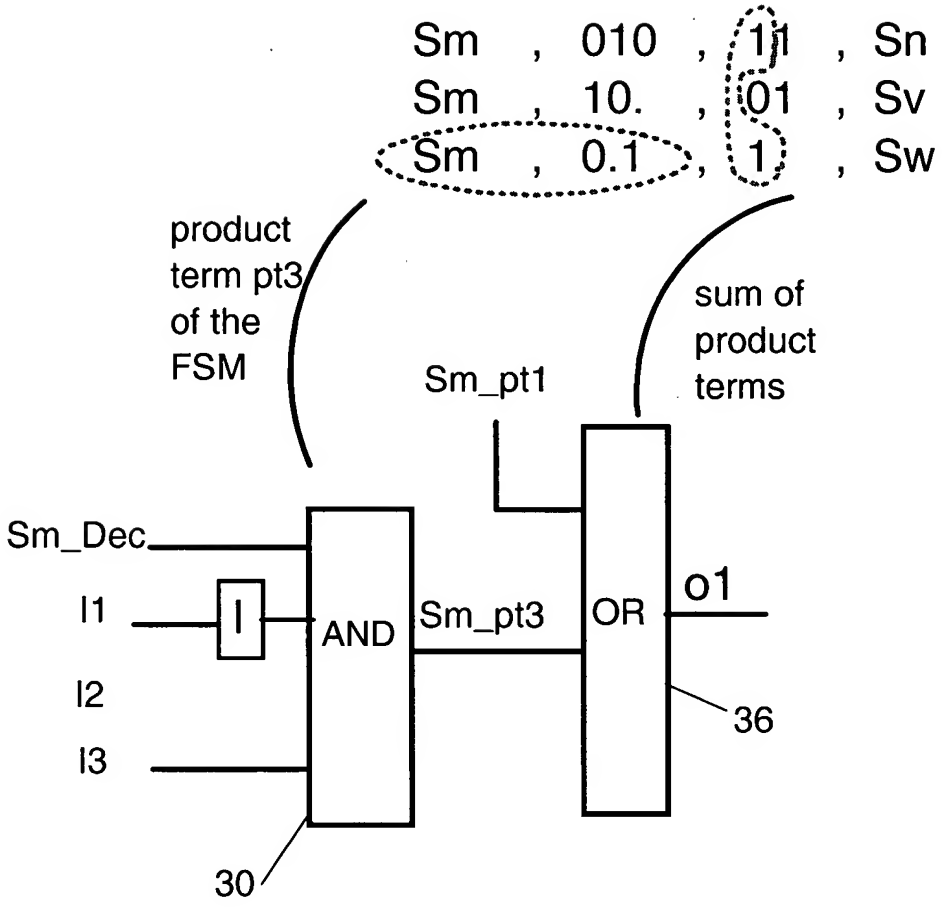

Sm , 010 , 11 , Sn
Sm , 10. , 01 , Sv
Sm , 0.1 , 1 , Sw
product term pt3 of the FSM
sum of product terms
Sm_pt1
Sm_Dec
I1
I2
I3
I
AND
Sm_pt3
OR
o1
36
30

FIG. 3

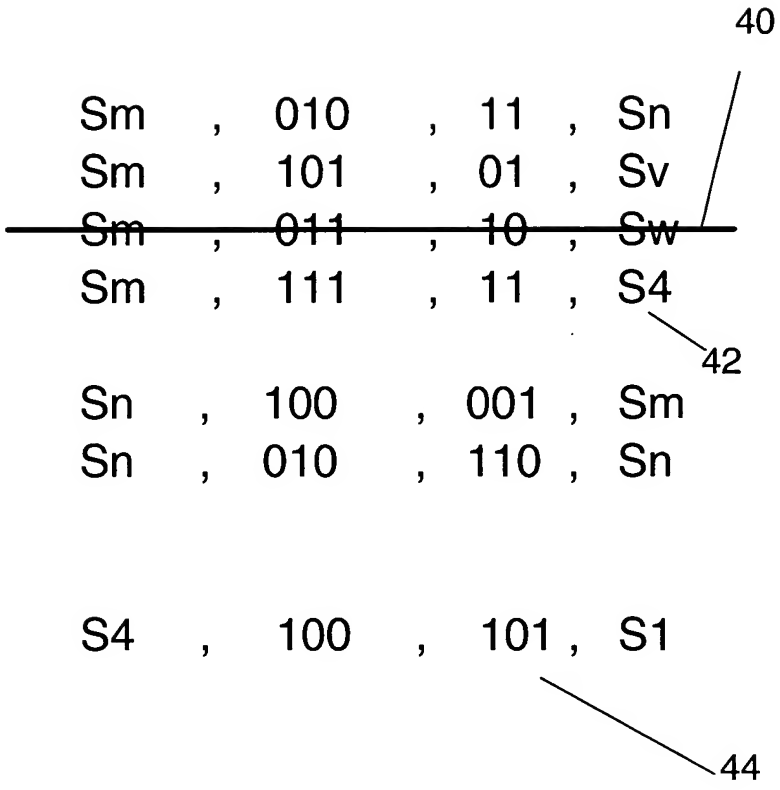

40
Sm , 010 , 11 , Sn
Sm , 101 , 01 , Sv
Sm , 011 , 10 , Sw
Sm , 111 , 11 , S4
42
Sn , 100 , 001 , Sm
Sn , 010 , 110 , Sn
S4 , 100 , 101 , S1
44

FIG. 4

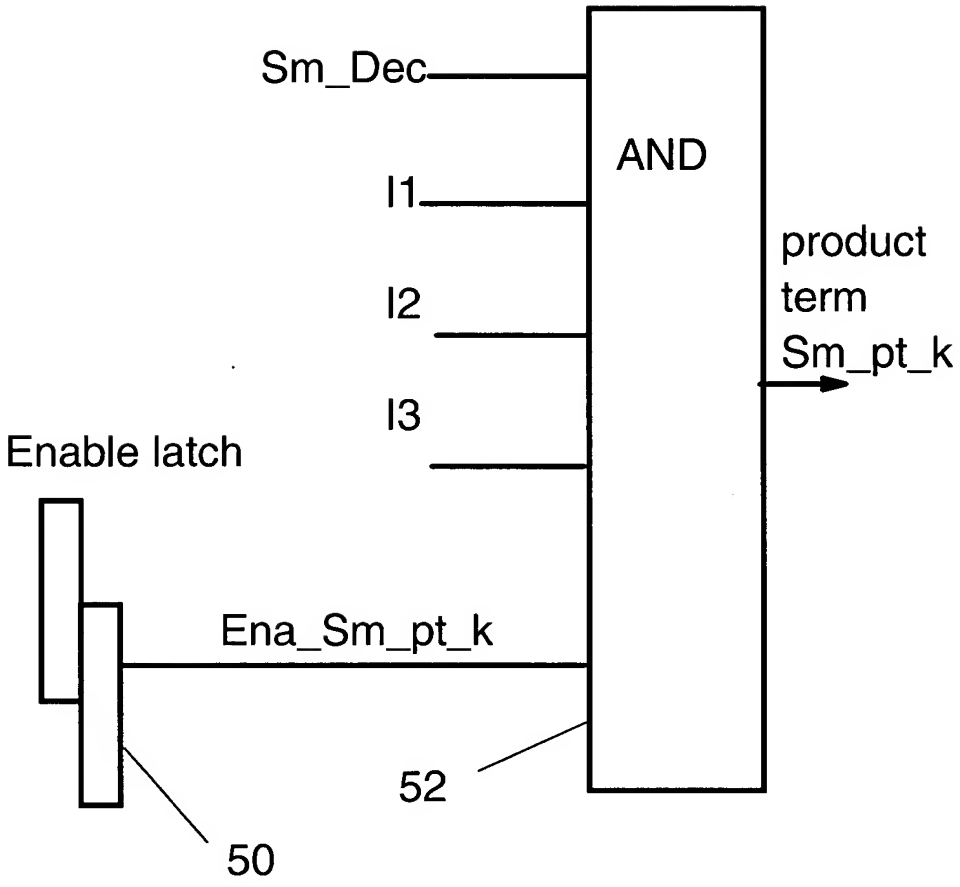

Sm_Dec
AND
I1
product
term
Sm_pt_k
I2
I3
Enable latch
Ena_Sm_pt_k
52
50

FIG. 5

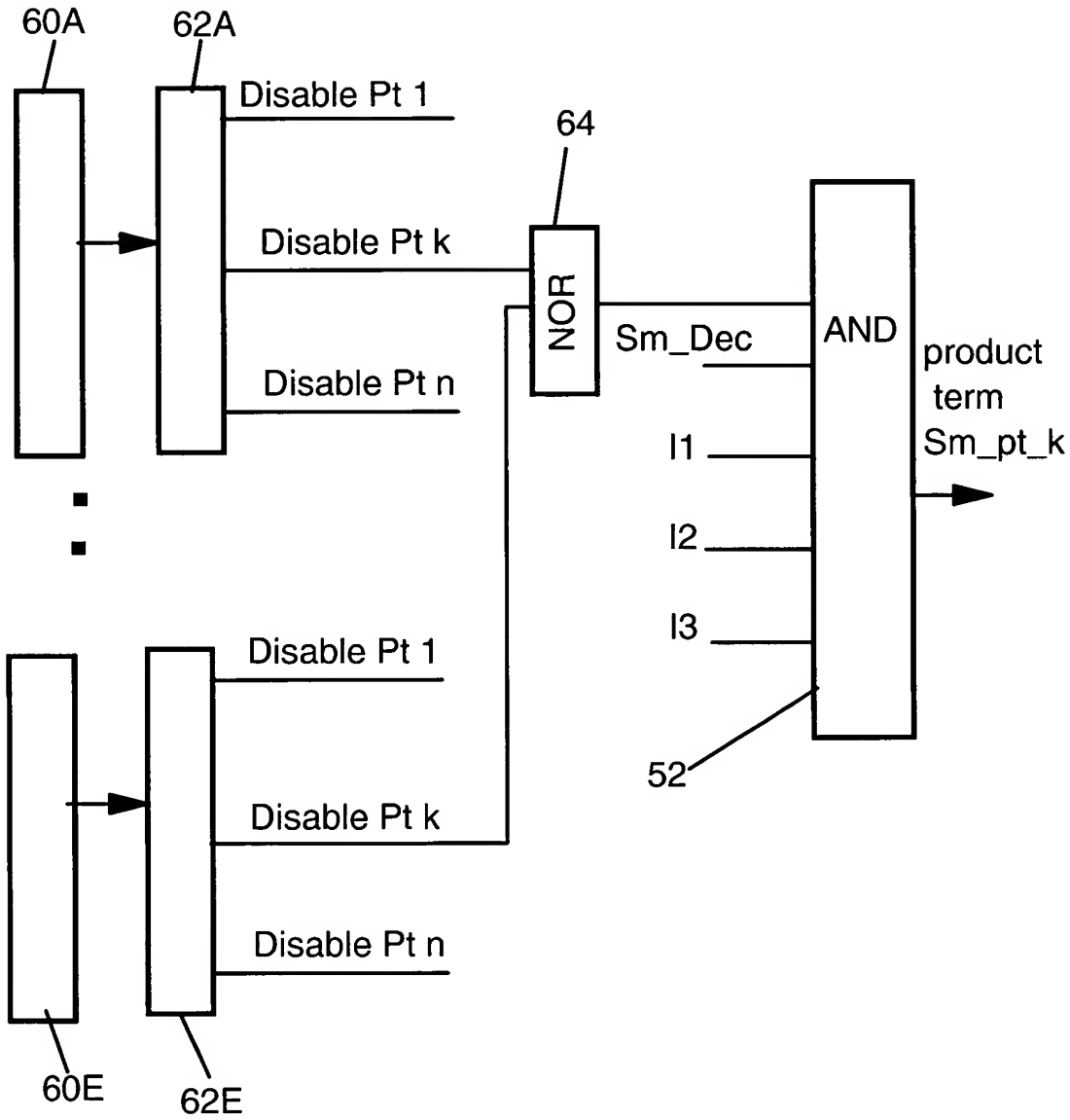

60A
62A
Disable Pt 1
64
Disable Pt k
NOR
Sm_Dec
AND
product
term
Sm_pt_k
Disable Pt n
I1
I2
I3
52
Disable Pt 1
Disable Pt k
Disable Pt n
60E
62E

FIG. 6

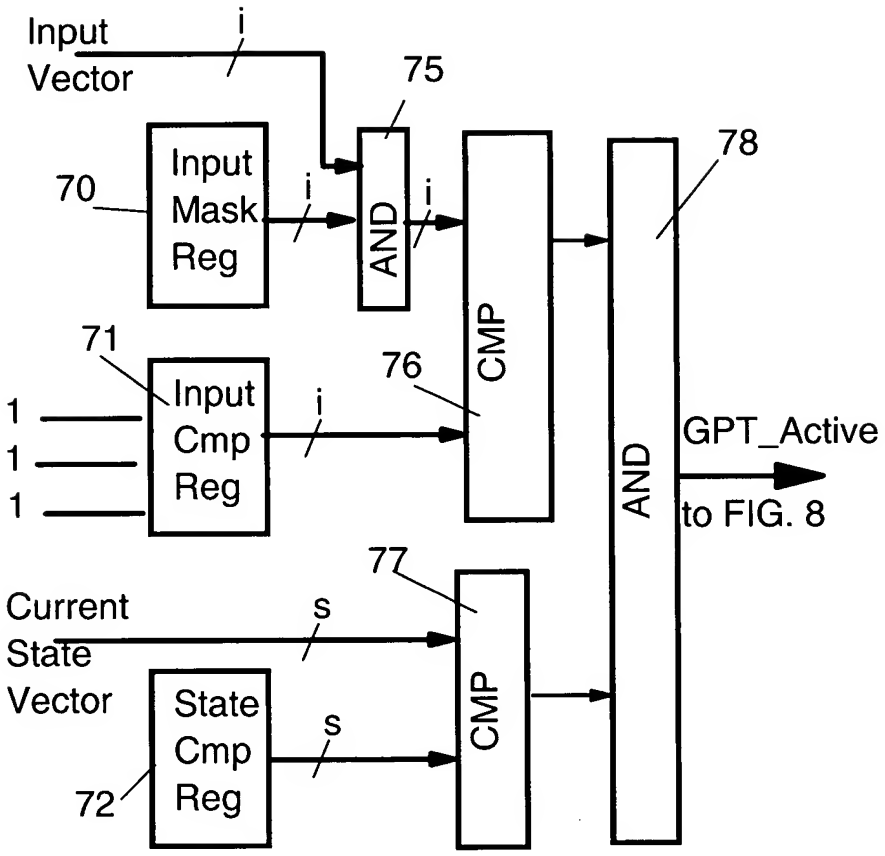

Input
Vector
i
75
78
70
Input
Mask
Reg
i
AND
i
CMP
71
76
Input
Cmp
Reg
1
1
1
i
AND
GPT_Active
to FIG. 8
77
Current
State
Vector
s
State
Cmp
Reg
72
s
CMP

FIG.7

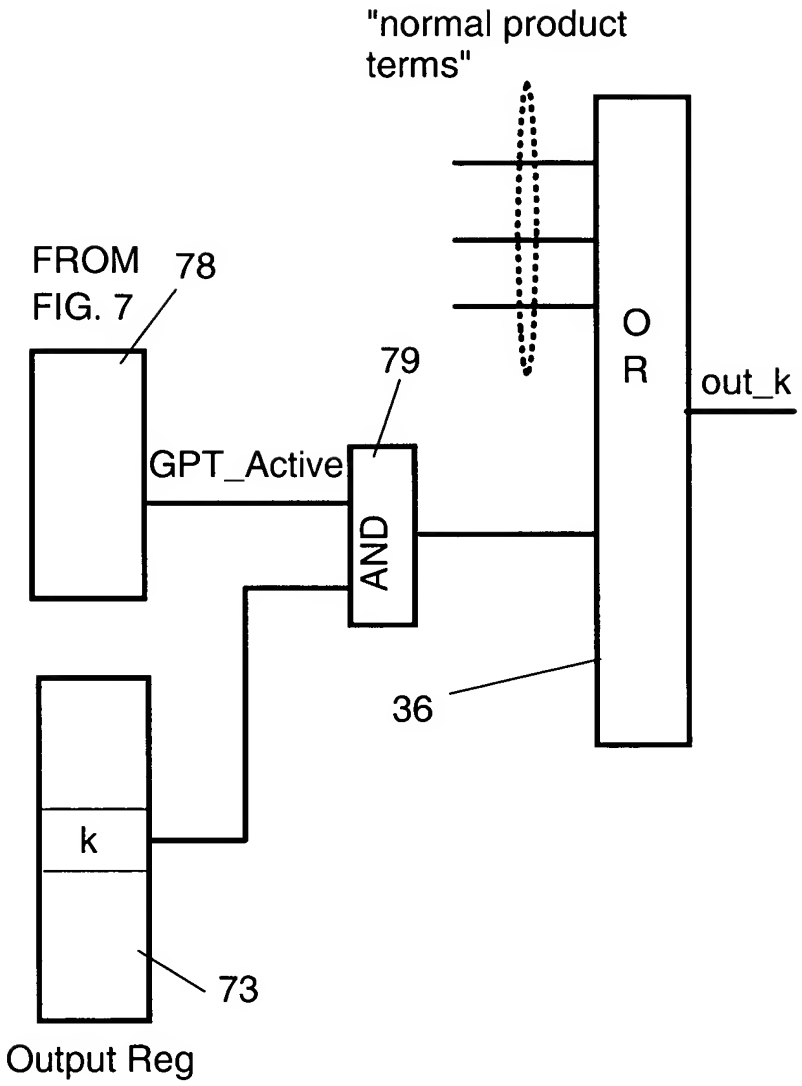

"normal product terms"
FROM FIG. 7
78
79
GPT_Active
AND
O R
out_k
36
k
73
Output Reg

FIG.8

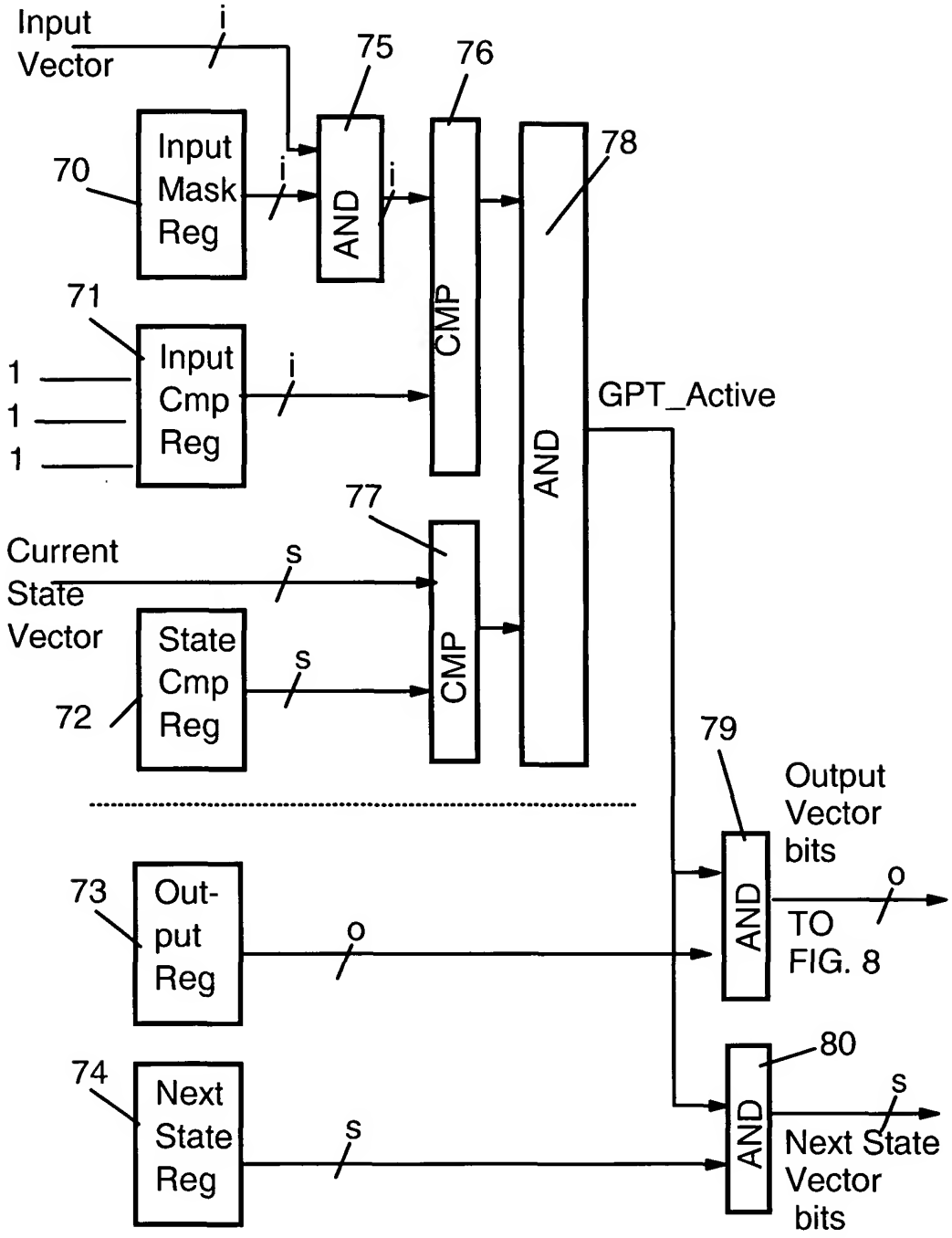

Input Vector
i
75
76
78
70
Input Mask Reg
i
AND
i
CMP
AND
71
Input Cmp Reg
1
1
1
i
GPT_Active
77
Current State Vector
s
State Cmp Reg
72
s
CMP
79
Output Vector bits
o
TO FIG. 8
73
Out-put Reg
o
AND
80
74
Next State Reg
s
s
Next State Vector bits
AND

FIG.8A

Sm_Pt1	Sm , 010	,	11 ,	Sn
Sm_Pt2	Sm , 10.	,	01 ,	Su
Sm_Pt3	Sm , 011	,	1. ,	Sv
	Sm , Otherwise	,	01 ,	Sw

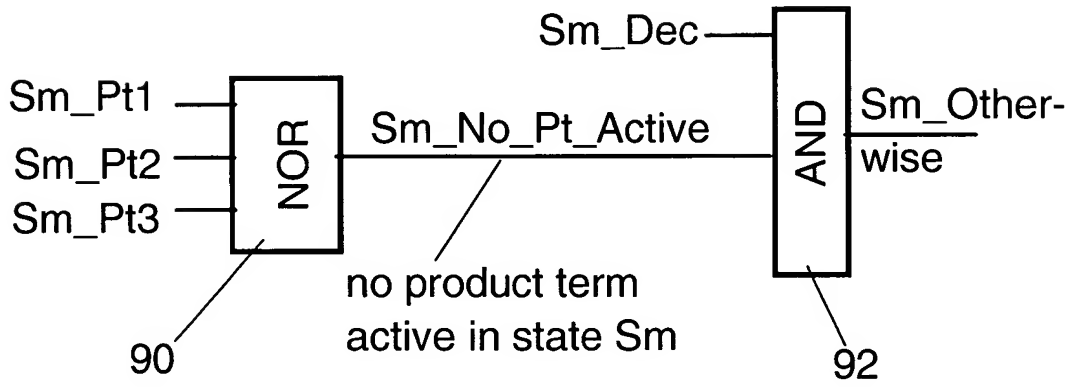


FIG.9
PRIOR ART

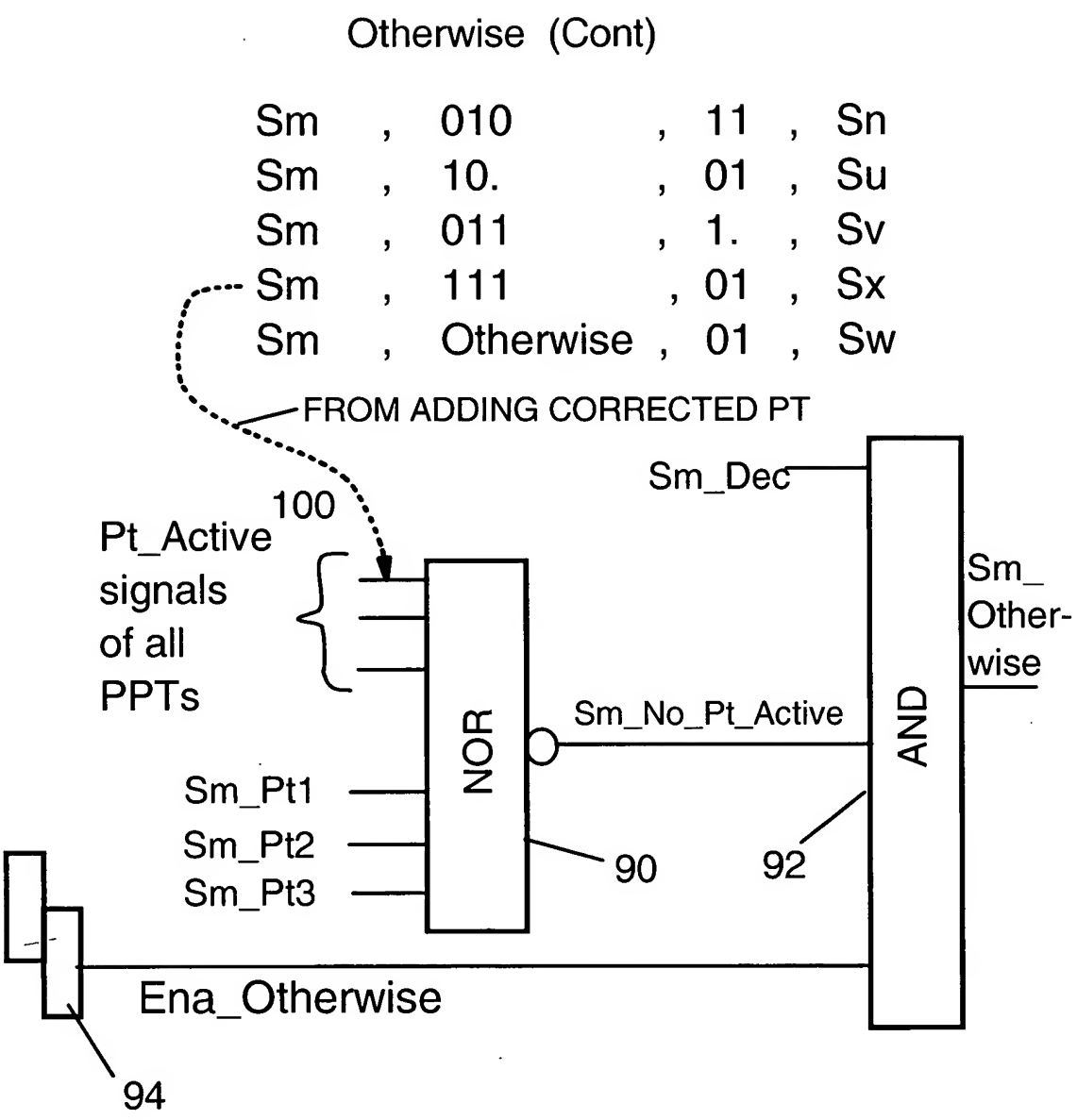

Otherwise (Cont)
Sm , 010 , 11 , Sn
Sm , 10. , 01 , Su
Sm , 011 , 1. , Sv
Sm , 111 , 01 , Sx
Sm , Otherwise , 01 , Sw
FROM ADDING CORRECTED PT
100
Pt_Active signals of all PPTs
Sm_Dec
Sm_ Other-wise
NOR
AND
Sm_No_Pt_Active
Sm_Pt1
Sm_Pt2
Sm_Pt3
90
92
Ena_Otherwise
94

FIG.10

A Programmable Otherwise

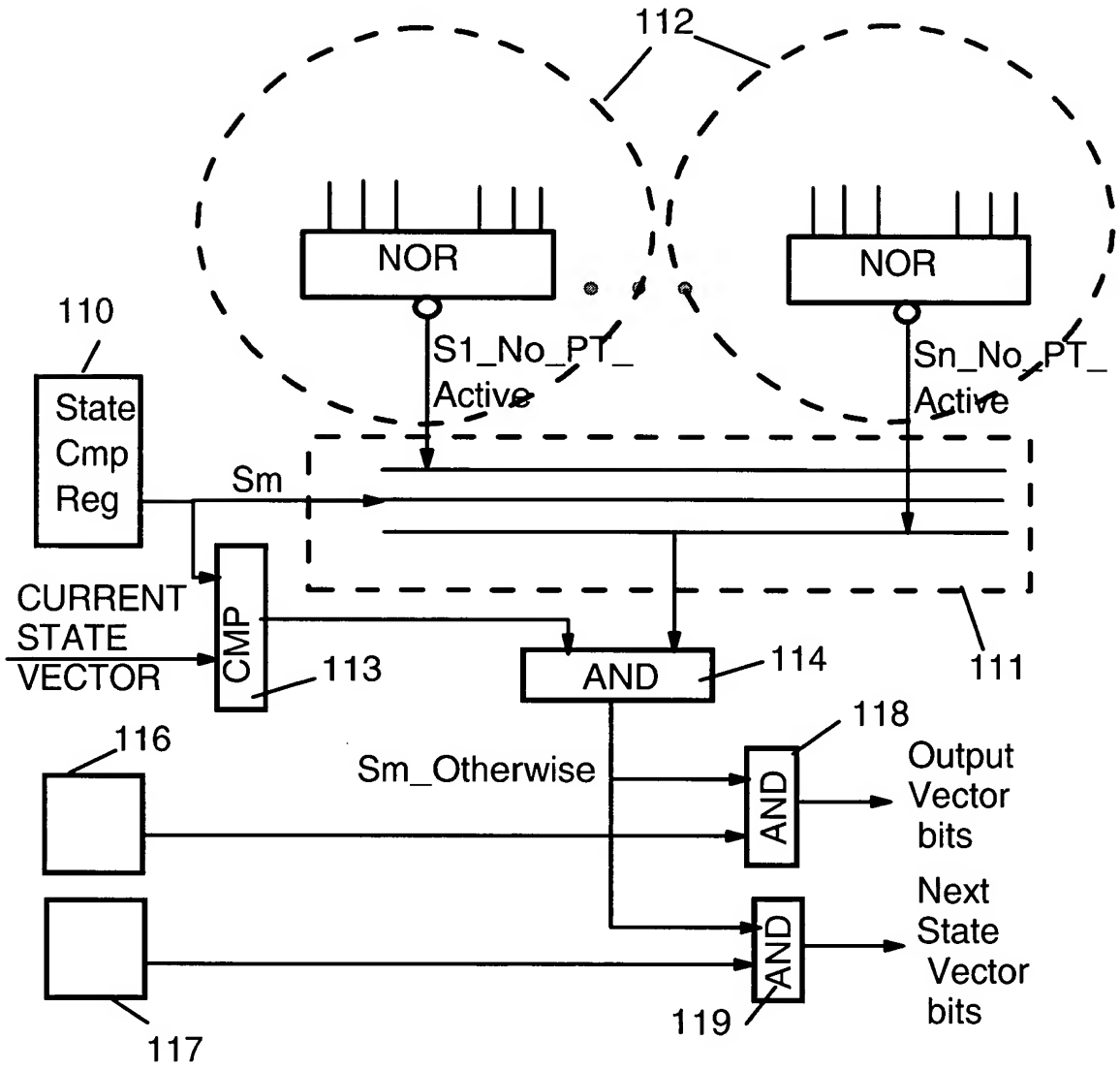


FIG.11

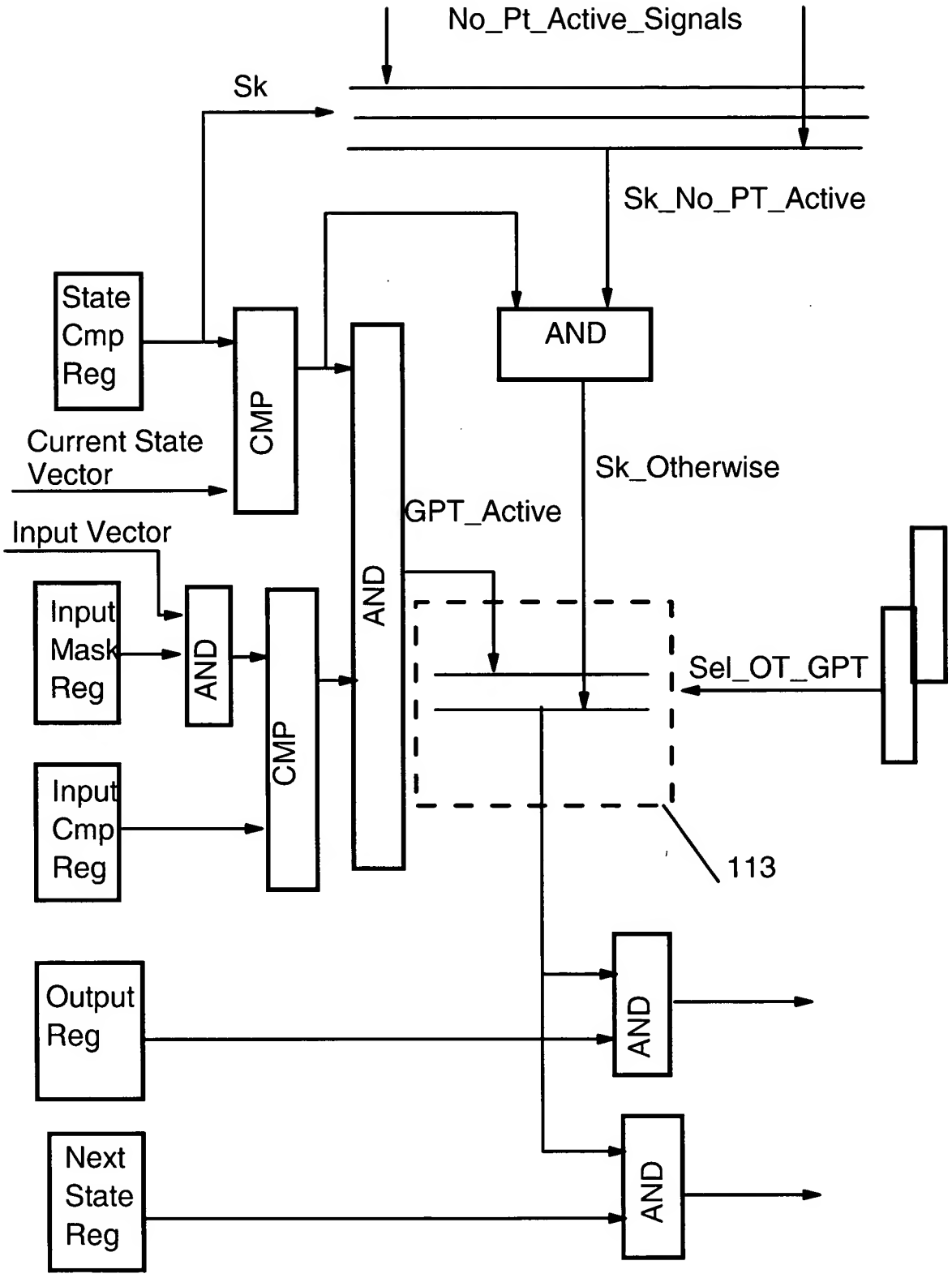
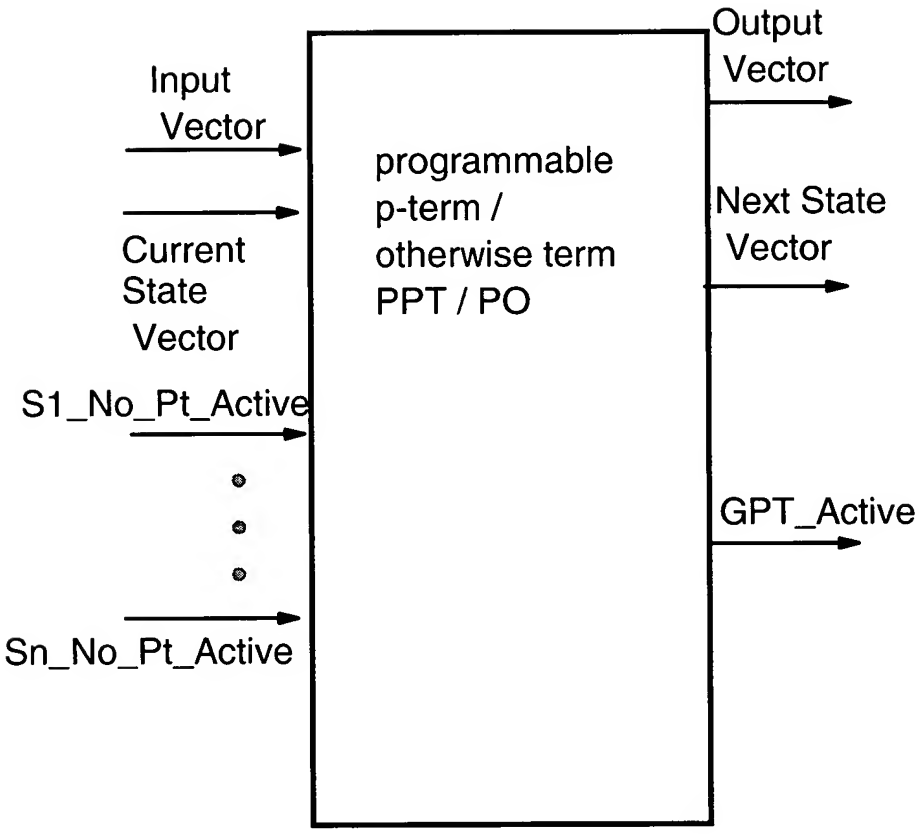

No_Pt_Active_Signals
Sk
Sk_No_PT_Active
State Cmp Reg
CMP
AND
Current State Vector
Sk_Otherwise
GPT_Active
Input Vector
Input Mask Reg
AND
AND
CMP
Sel_OT_GPT
Input Cmp Reg
113
Output Reg
AND
Next State Reg
AND

FIG.12



The I/Os of a programmable PO-term

FIG.13

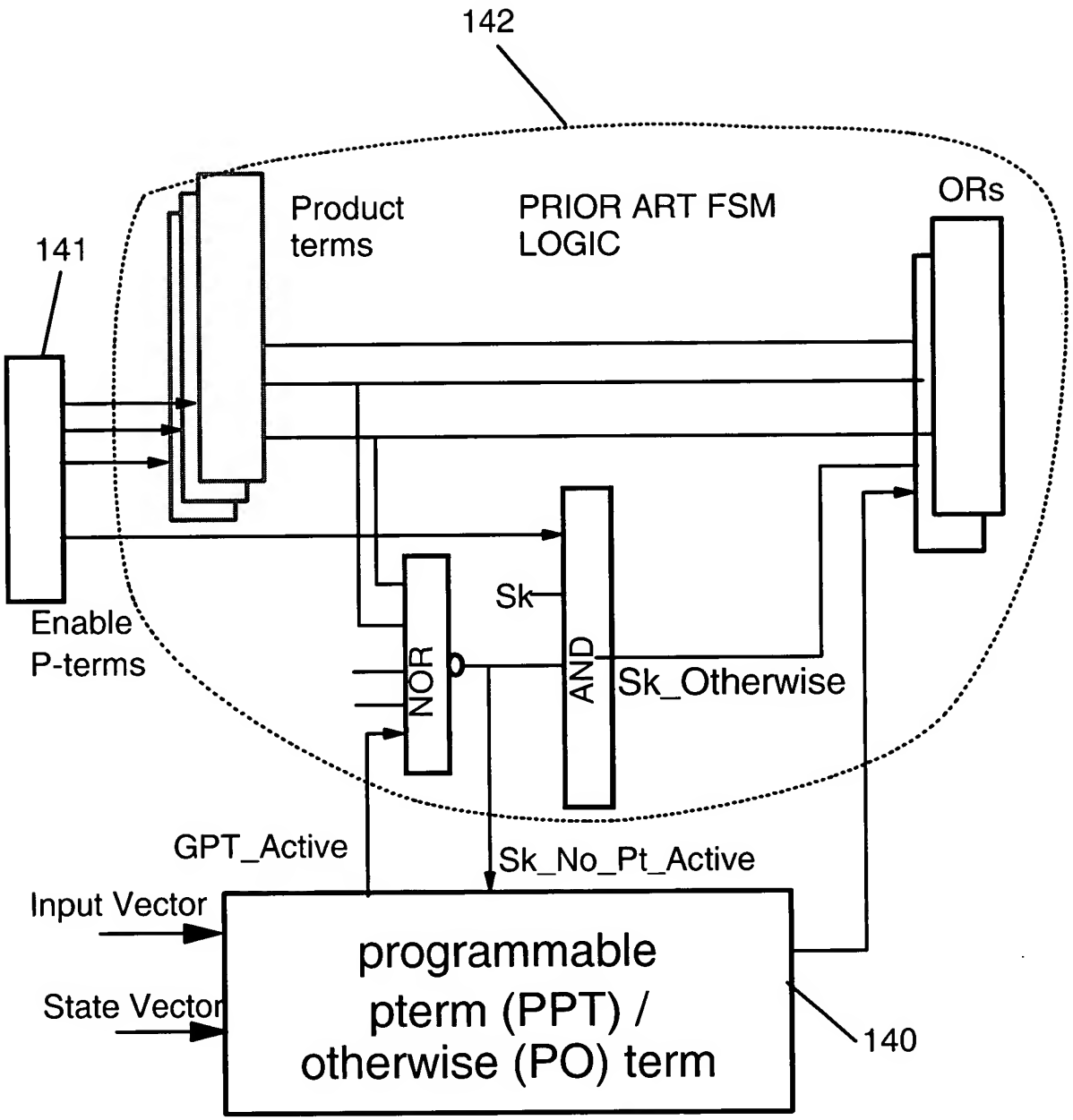

142
141
Product terms
PRIOR ART FSM LOGIC
ORs
Enable P-terms
Sk
NOR
AND
Sk_Otherwise
GPT_Active
Sk_No_Pt_Active
Input Vector
State Vector
programmable pterm (PPT) / otherwise (PO) term
140

FIG.14

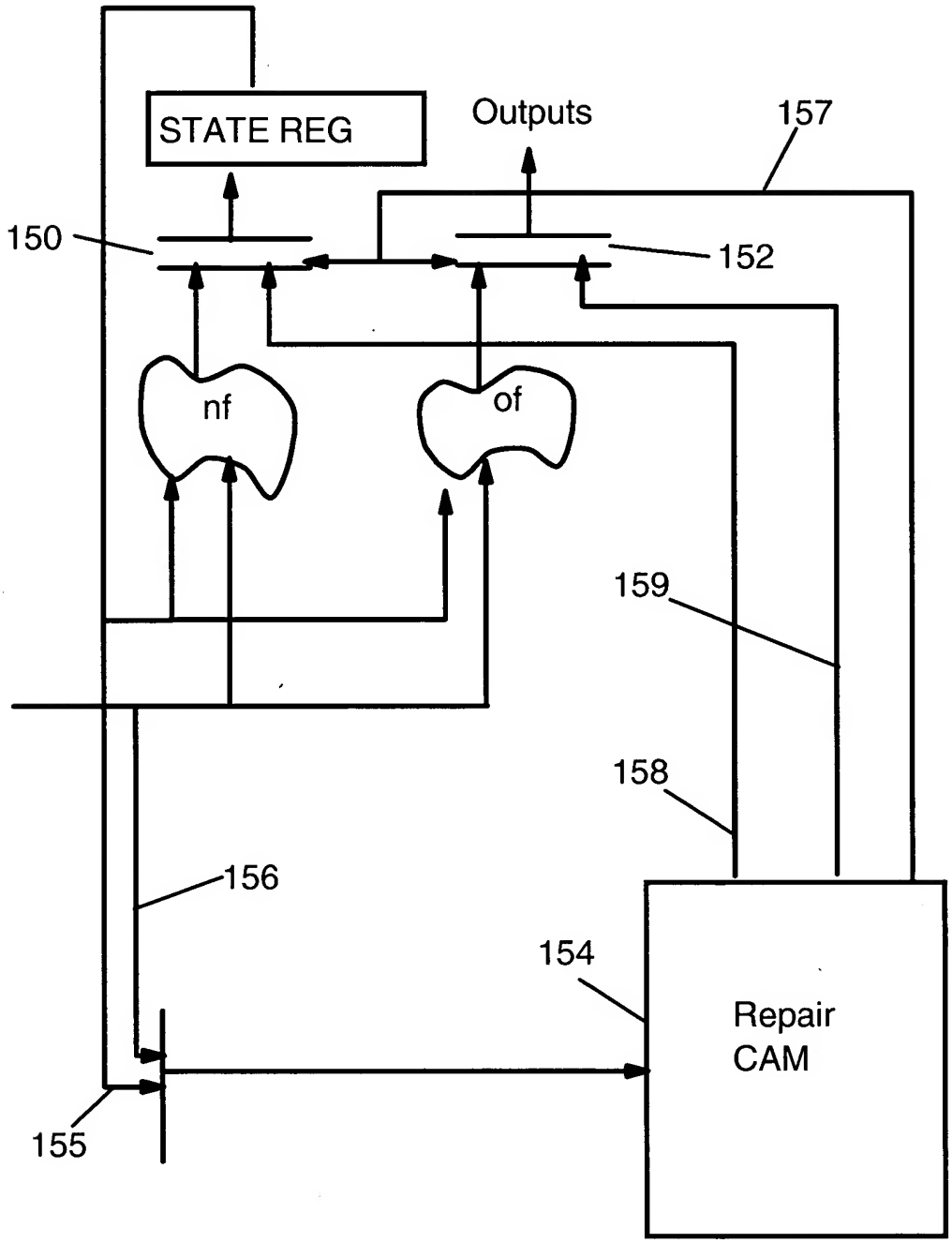

STATE REG
Outputs
157
150
152
nf
of
159
158
156
154
Repair
CAM
155

FIG.15

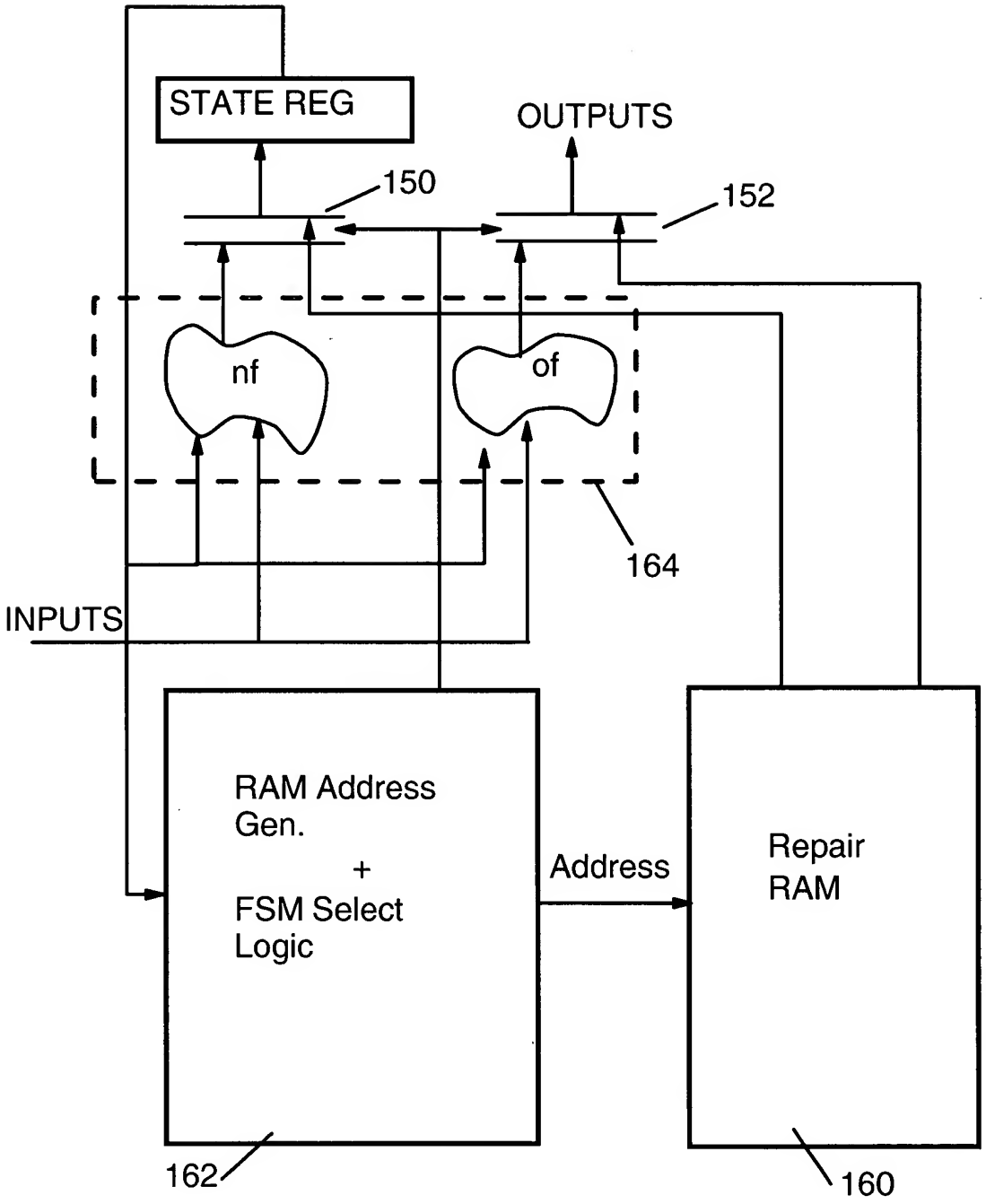

STATE REG
OUTPUTS
150
152
nf
of
164
INPUTS
RAM Address
Gen.
+
FSM Select
Logic
Address
Repair
RAM
162
160

FIG.16

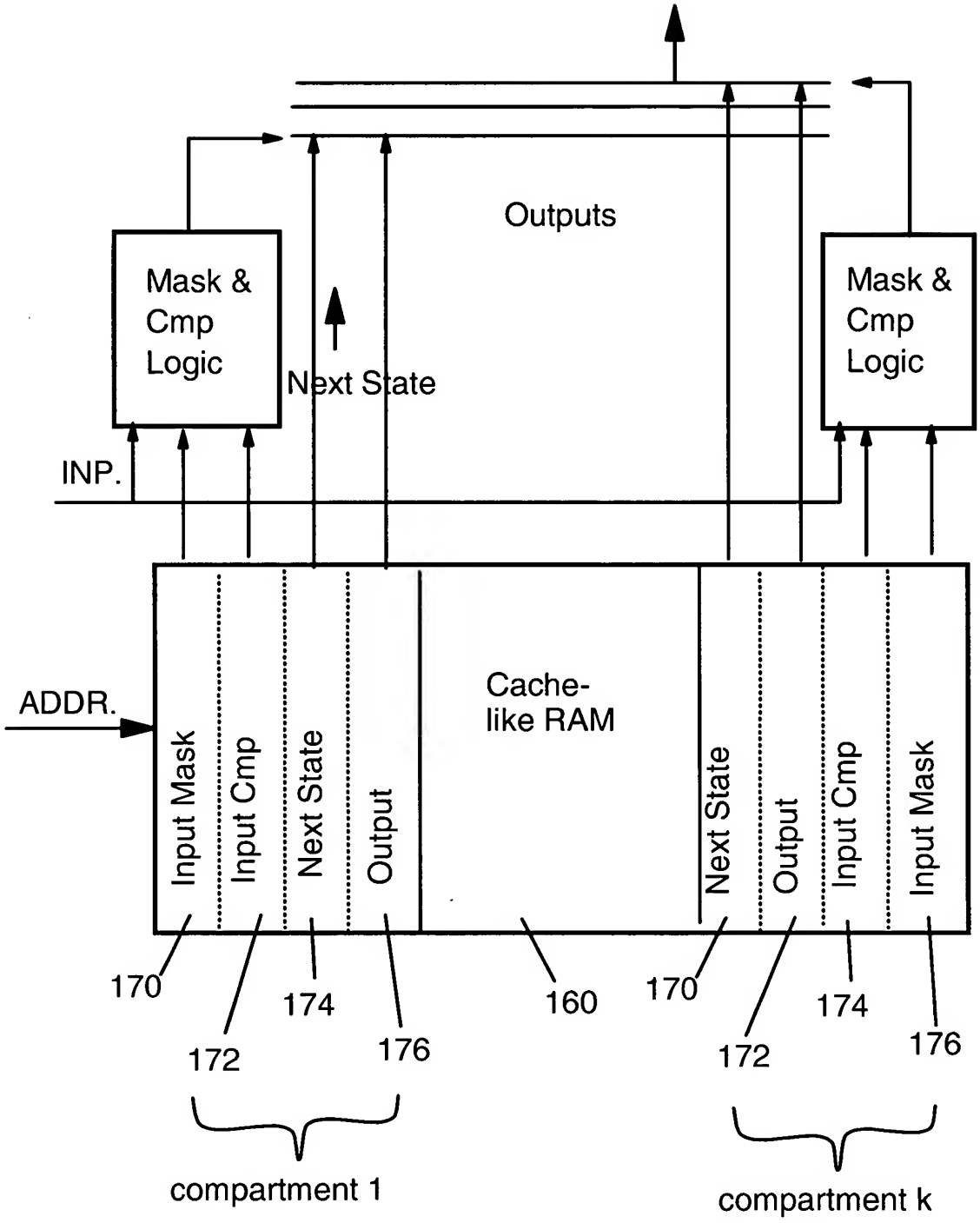

Outputs
Mask &
Cmp
Logic
Next State
Mask &
Cmp
Logic
INP.
ADDR.
Input Mask
Input Cmp
Next State
Output
Cache-
like RAM
Next State
Output
Input Cmp
Input Mask
170
172
174
176
160
170
172
174
176
compartment 1
compartment k

FIG.17

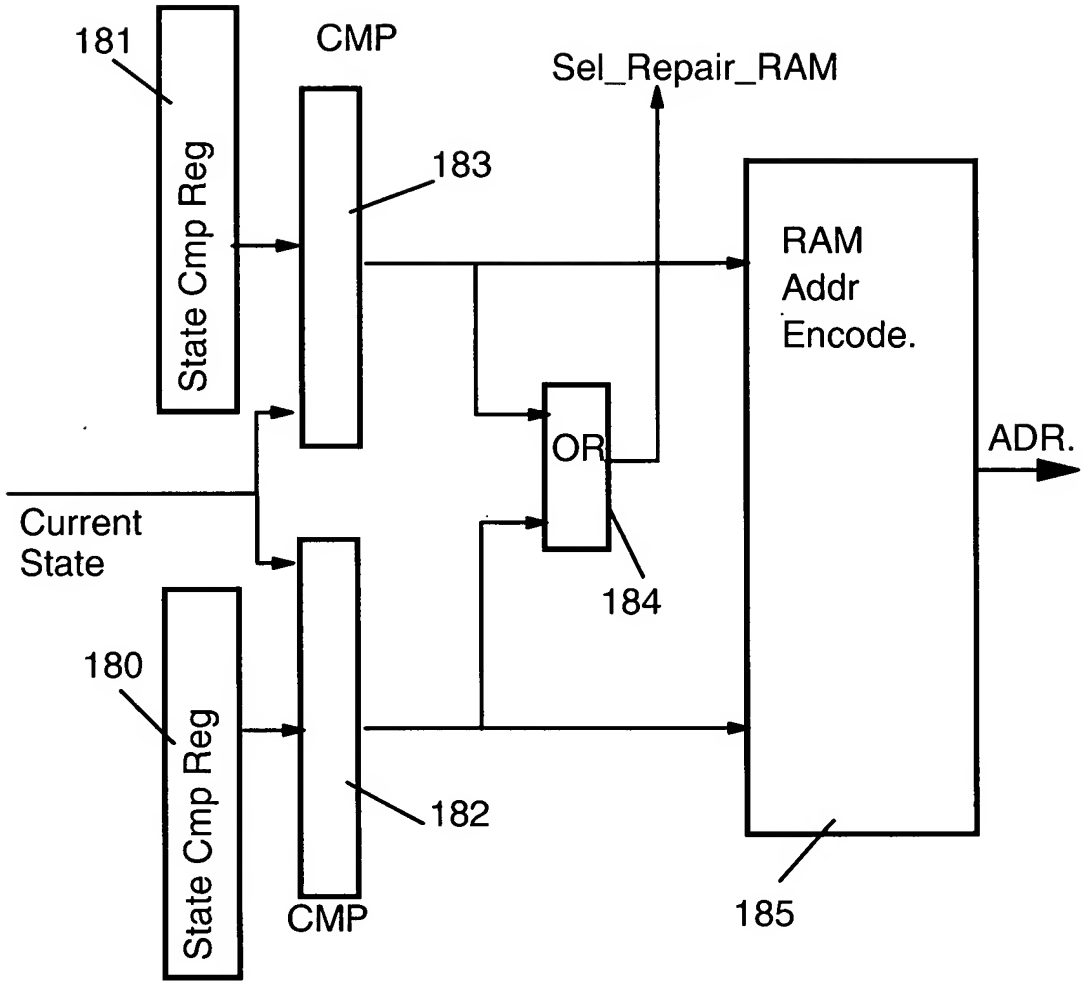

181
State Cmp Reg
CMP
183
Sel_Repair_RAM
RAM
Addr
Encode.
ADR.
OR
184
Current
State
180
State Cmp Reg
182
CMP
185

FIG.18